

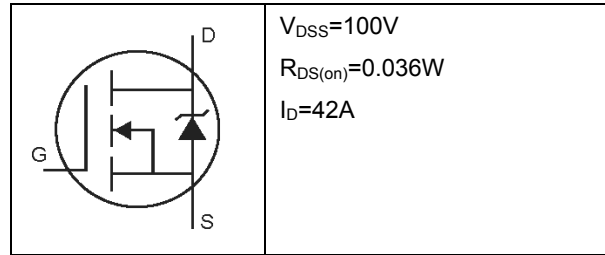
FEATURES

- Avalanche Process Technology
- Dynamic dv/dt Rating
- 175 Operating Temperature
- Fast Switching
- Fully Avalanche Rated

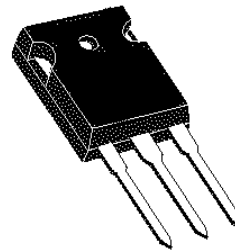
Description

Fifth Generation HEXFETs from Artschip utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-3P



TO-247AC

Absolute Maximum Ratings

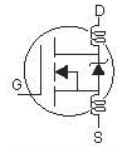
	Parameter	Max.	Units
I_D @ $T_c=25$	Continuous Drain Current, V_{GS} @10V	42	A
I_D @ $T_c=100$	Continuous Drain Current, V_{GS} @10V	30	
I_{DM}	Pulsed Drain Current	140	
P_D @ $T_c=25$	Power Dissipation	160	W
	Linear Derating Factor	1.1	W/
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy	420	mJ
I_{AR}	Avalanche Current	22	A
E_{AR}	Repetitive Avalanche Energy	16	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

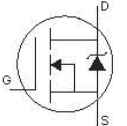
	Parameter	Typ.	Max.	Units
R_{QJC}	Junction-to-Case	-	0.95	/W
R_{QCS}	Case –to-Sink, Flat, Greased Surface	0.24	-	
R_{QJA}	Junction-to-Ambient	-	40	

Electrical Characteristics @ $T_J=25$ (Unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$DV_{(BR)DSS}/DT_J$	Breakdown Voltage Temp. Coefficient	-	0.11	-	V/	Reference to 25 , $I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	-	-	0.036	W	$V_{GS}=10V, I_D=23A$
g_{fs}	Forward Transconductance	2.0	-	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	-	-	25	μA	$V_{DS}=100V, V_{GS}=0V$
		-	-	250		$V_{DS}=80V, V_{GS}=0V, T_J=150$
I_{GSS}	Gate-to-Source Forward Leakage	-	-	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	-	-	-100		$V_{GS}=-20V$
Q_g	Total Gate Charge	-	-	110	nC	$I_D=22A$
Q_{gs}	Gate-to-Source Charge	-	-	15		$V_{DS}=80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	-	-	58		$V_{GS}=10V$, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	-	11	-	ns	$V_{DD}=50V$ $I_D=22A$ $R_G=3.6W$ $R_D=2.9W$, See Fig. 10
t_r	Rise Time	-	56	-		
$t_{d(off)}$	Turn-Off Delay Time	-	45	-		
t_f	Fall Time	-	40	-		
L_D	Internal Drain Inductance	-	5.0	-	nH	Between lead, 6mm (0.25in.) From package And center of die contact
L_S	Internal Source Inductance	-	13	-		
C_{iss}	Input Capacitance	-	1900	-	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$, See Fig.5
C_{oss}	Output Capacitance	-	450	-		
Cr_{ss}	Reverse Transfer Capacitance	-	230	-		


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	-	-	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	-	-	140		
V_{SD}	Diode Forward Voltage	-	-	1.3	V	$T_J=25$, $I_S=23A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	-	180	270	ns	$T_J=25$, $I_F=22A$
Q_{rr}	Reverse Recovery Charge	-	1.2	1.8	μC	$di/dt=100A/\mu s$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				


Notes:

Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)

Starting $T_J=25$, $L=1.7mH$

$R_G=25W, I_{AS}=22A$. (See Figure 12)

$I_{SD}\leq 40A, di/dt\leq 180A/\mu s, V_{DD}\leq V_{(BR)DSS}, T_J\leq 175$

Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

Uses IRF1310N data and test conditions

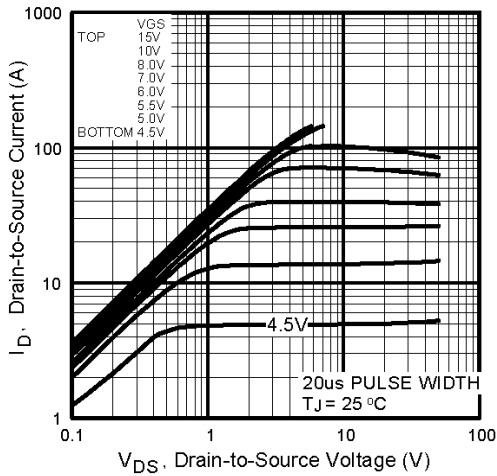


Fig 1. Typical Output Characteristics

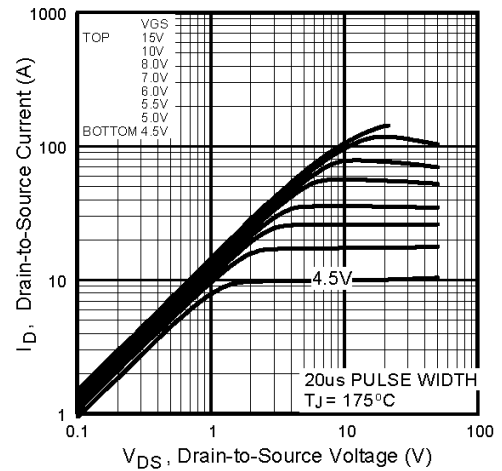


Fig 2. Typical Output Characteristics

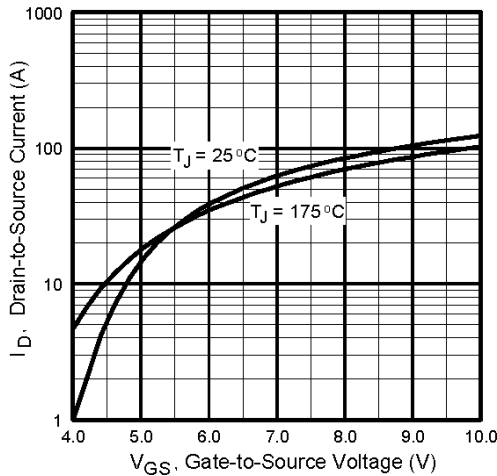


Fig 3. Typical Transfer Characteristic

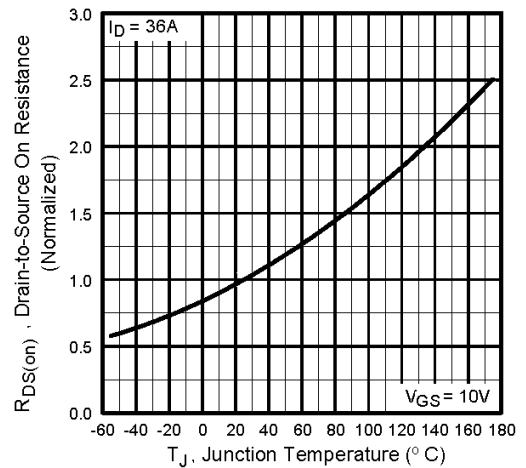


Fig 4. Normalized On-Resistance Vs. Temperature

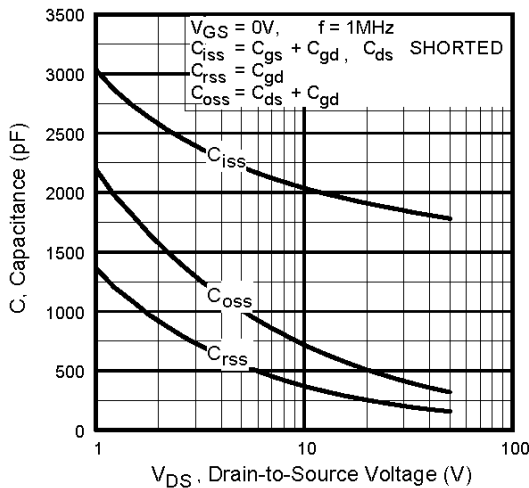


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

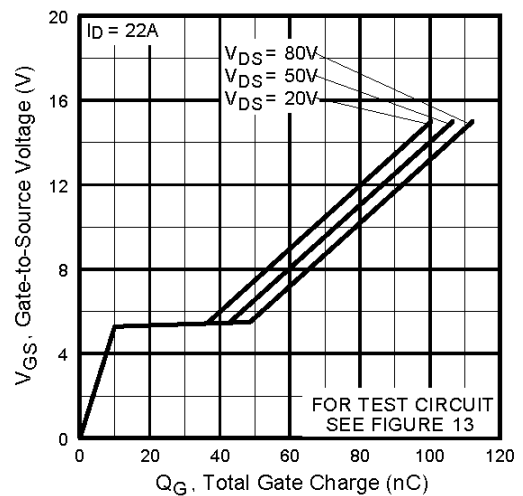


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

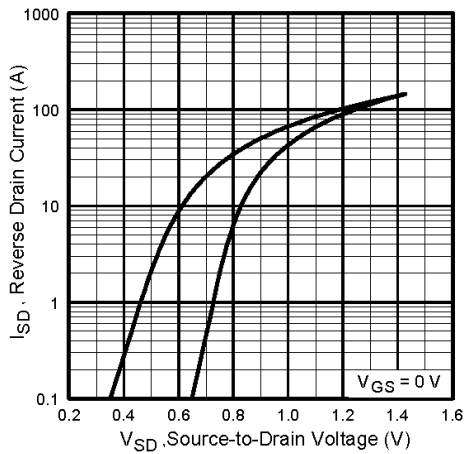


Fig 7. Typical Source –Drain Diode Forward Voltage

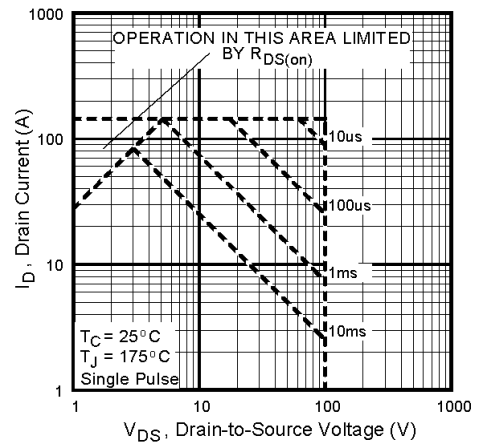


Fig 8. Maximum Safe Operating Area

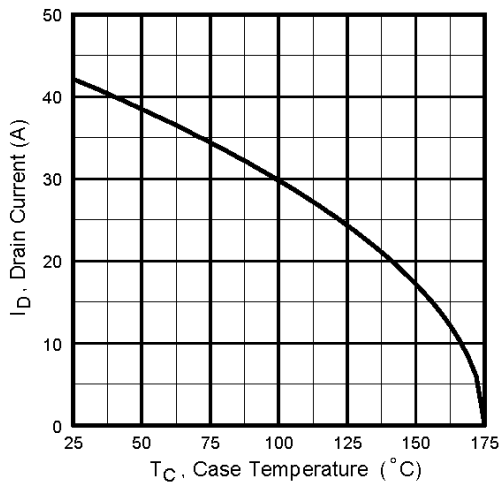


Fig 9. Maximum Drain Current Vs. Case Temperature

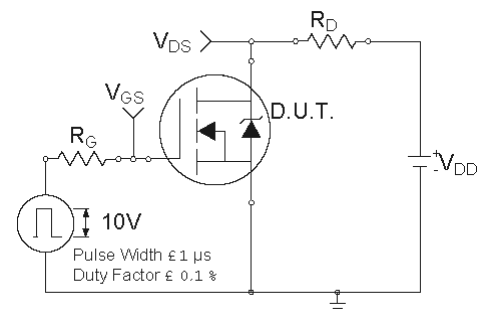


Fig 10a. Switching Time Test Circuit

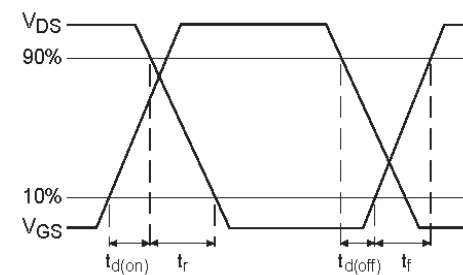


Fig 10b. Switching Time Waveforms

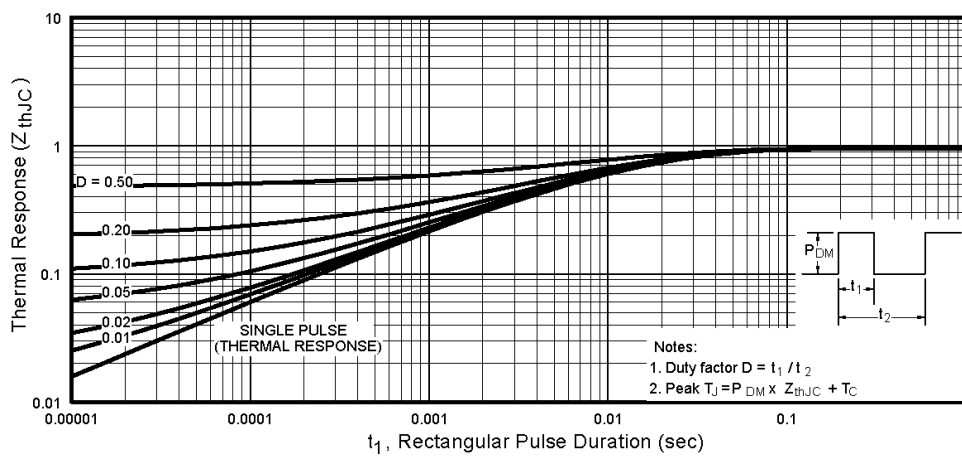


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

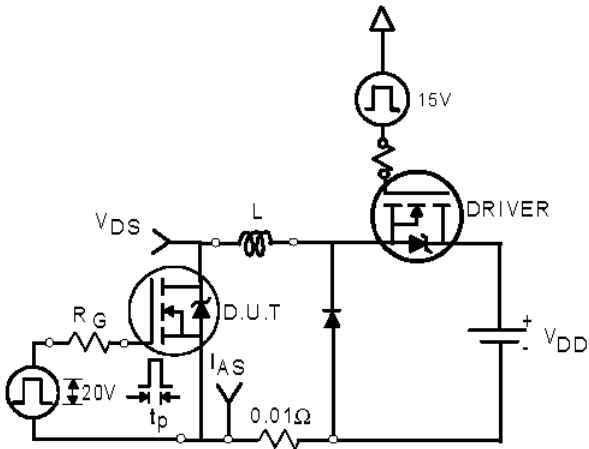


Fig 12a. Unclamped Inductive Test Circuit

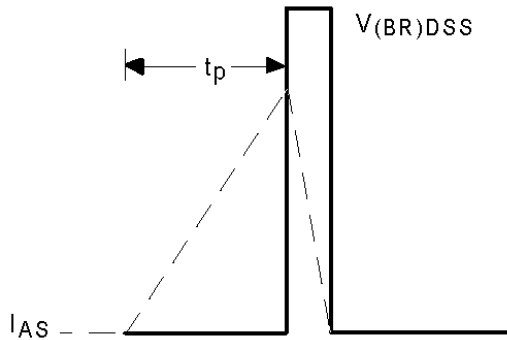


Fig 12b. Unclamped Inductive Waveforms

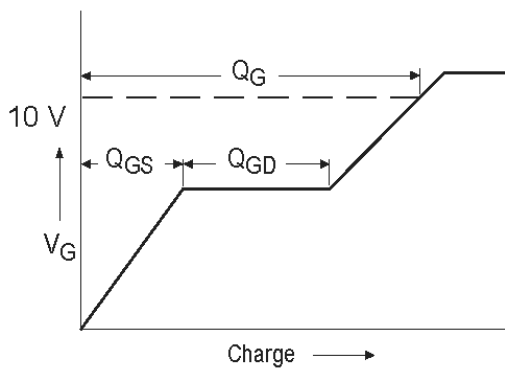


Fig 13a. Basic Gate Charge Waveform

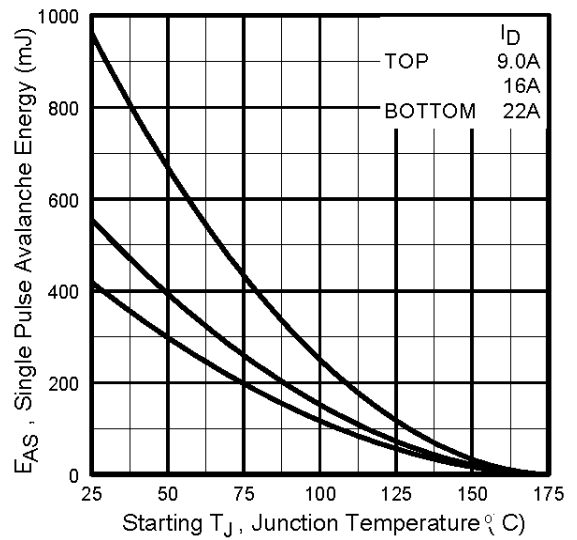


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

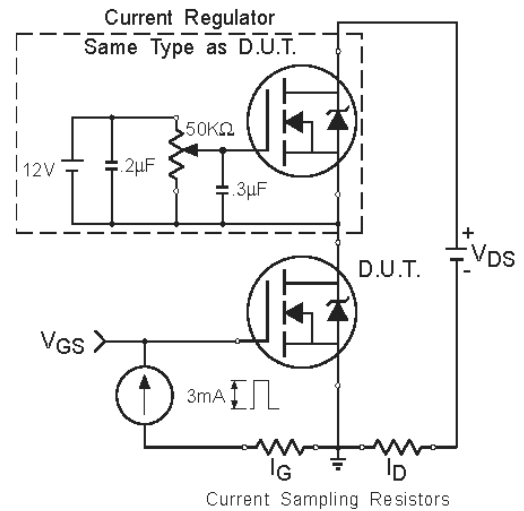
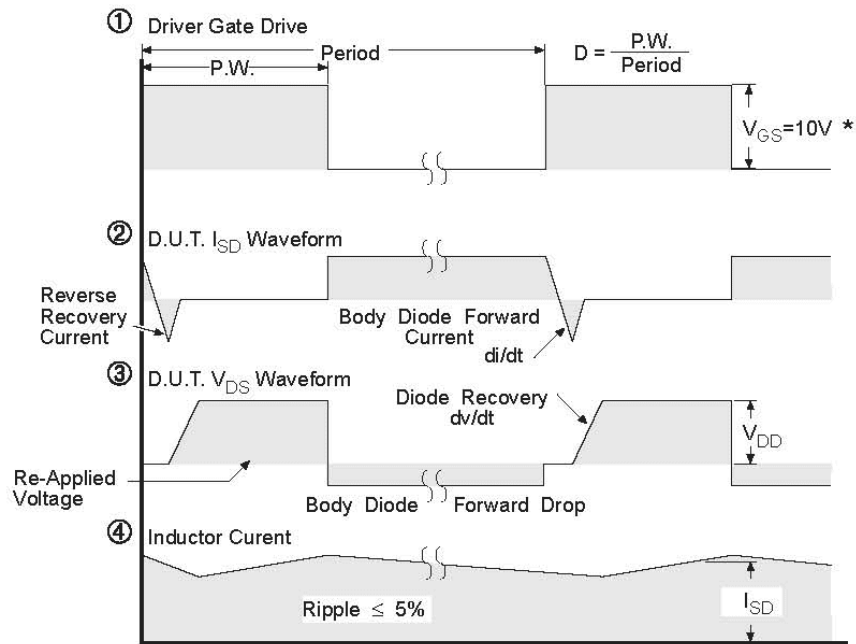
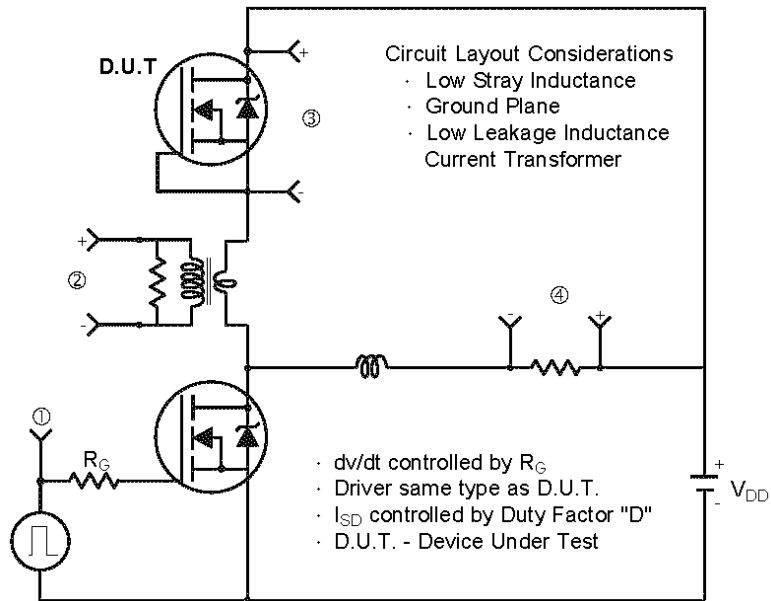


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



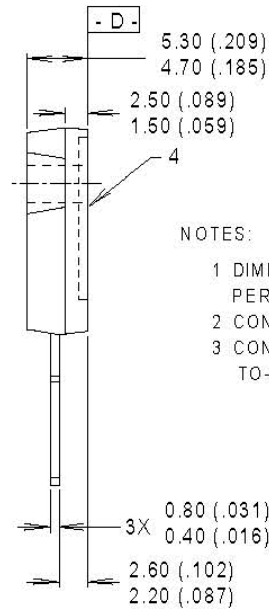
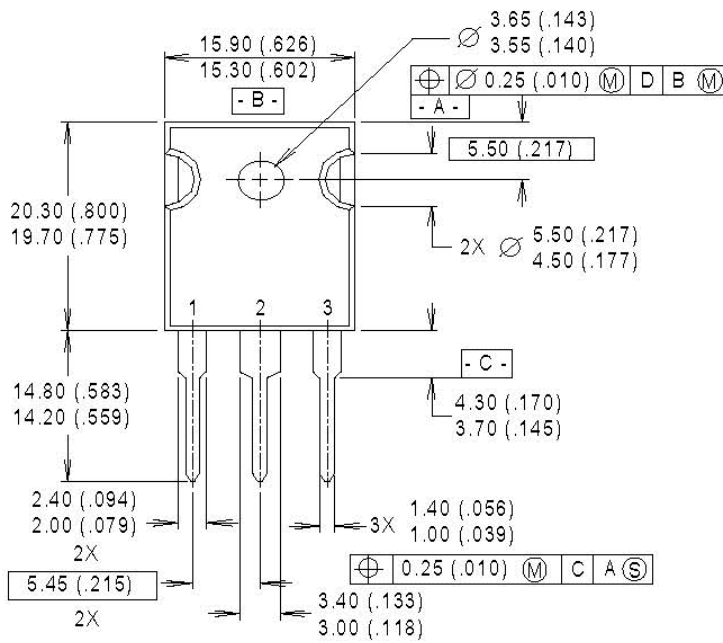
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

To-247AC Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN